THERMAL RESISTANCE, POWER DISSIPATION and CURRENT RATING for CERAMIC and PORCELAIN MULTILAYER CAPACITORS

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INTRODUCTION

The information in this article makes it possible for a circuit designer to calculate the temperature rise of any multilayer capacitor*. The method used for calculation of the temperature rise of a capacitor is quite similar to the techniques that are universally used for transistors.

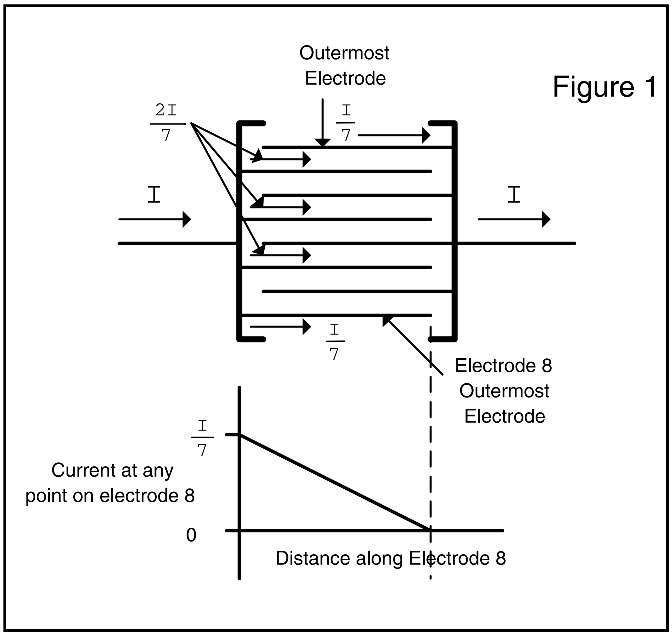
The theoretical determination of the temperature rise of a capacitor due to AC current flowing through it is a difficult task. Equipment designers, when faced with the problem, require parameters that are generally not available from the capacitor manufacturer, such as ESR (Equivalent Series Resistance), and Θ (Thermal Resistance), etc., of the capacitor.

If the ESR and current are known, the power dissipation and thus, the heat generated in the capacitor can be calculated. From this, plus the thermal resistance of the capacitor and its external connections to a heat sink, it becomes possible to determine the temperature rise above ambient of the capacitor.

Current distribution is not uniform throughout a monolithic capacitor, since the outermost plates (electrodes) carry less current than the inner electrodes. This is shown in Figure 1 for an 8 electrode capacitor. From the figure, it can be seen that there are 7 capacitor section's (Since for N electrodes there (N-1) capacitor sections). If the total current into the capacitor is I, the current for each section is $I/7$. For an outermost electrode, $I/7$ is actually the current carried by the electrode. For all other electrodes, the current is 2 ($I/7$) since the electrodes carry the current for two sections. Furthermore, the current is not the same at each point on the electrode. For electrode 8, the current is $I/7$ at the left or termination end and zero at the right or open end. The current distribution is approximately as shown in Figure 1. As a result of this current distribution, the heat generated is not uniform within the capacitor.

For an actual multilayer capacitor, there are connection resistances between the electrodes and the terminations, which cause heat generation. This effect depends upon the quality of manufacture of the capacitor. Some manufactures have fairly high connection resistances, whereas others have connection resistances that are undetectable.

This article assumes a capacitor manufactured with no defects, i.e. zero connection resistances, and it also assumes that the temperature difference across the thickness of the dielectric between the electrodes is negligible, i.e. less than 1°C.



The validity of the assumptions has been checked experimentally by measurements of ESR and temperature rise vs. RF current for various capacitor values at a frequency of 30 MHz.

CAPACITOR RF CURRENT RATINGS

There are two criteria for maximum current rating.

The first criterion is due to the rated working voltage of the capacitor and is discussed below.

The RF current corresponding to this voltage is:

$$I_p = \frac{V_{peak} - V_{DC}}{X_C} \qquad (1)$$

where,

Ip = Peak RF current

V_{peak} = *Rated Working voltage* of the capacitor

V_{DC} = DC Voltage across the capacitor

X_C = Reactance of the capacitor at frequency of operation

*Manufactured by American Technical Ceramics Corp.

The RF current must not exceed the value from Equation (1).

The second criterion is due to the temperature rise caused by power dissipation, (discussed in succeeding paragraphs). In most applications, multilayer capacitors are soldered into the circuit or fastened into place by use of a conductive epoxy. Since the maximum temperature of the solder normally used on the terminations of the capacitor is 190° C; 125° C was chosen as the maximum for one series of capacitors.* This ensures the user that the temperature will not exceed the softening temperature of the epoxy or solder. This temperature then determines the maximum power dissipation and in turn, the maximum current, if the capacitor ESR is known.

WORKING VOLTAGE RATING

The criterion for the maximum voltage rating depends upon the voltage breakdown characteristics of the capacitor. The voltage breakdown rating is normally some fraction of the actual internal breakdown voltage. For one series of porcelain dielectric capacitors,** the breakdown voltage exceeds 1000 volts/mil of dielectric thickness and is virtually independent of temperature. Other dielectrics, such as barium titaniate and many NPO's have much lower breakdown voltages/mil.

In some situations, the surface breakdown or flash-over voltage rather than the actual internal breakdown voltage is the determining factor. In these cases, the flash-over determines the rated working voltage. The factors affecting flash-over voltage include surface length of path, surface contamination and environmental conditions.

CURRENT RATING DUE TO POWER DISSIPATION

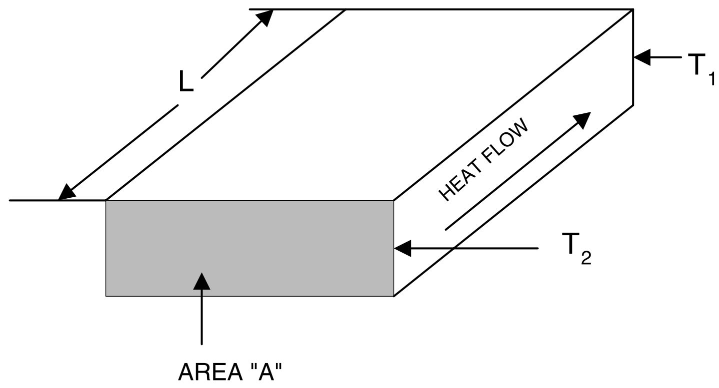
Before launching into a thermal analysis of the multilayer capacitor, it is advisable to review some basic thermal principles:

HEAT TRANSFER

The equivalent of Ohm's Law for heat transfer is: (See Figure 2.)

$$Pd = \frac{(T2 - T1)}{\Theta} \qquad \text{(Watts)} \qquad (2)$$

Figure 2.



where,

A = Cross section plane perpendicular to heat (cm²)

P_d = Power dissipated (watts) at area "A"

T_2 = Temperature (°C) of cross section area "A" (perpendicular to heat flow)

T_1 = Temperature (°C) at a cross section area at a distance L from area "A"

L = Length of path (cm) between areas

Θ = Thermal resistance of path across length L (°C/W)

where, Pd is analogous to electrical current, $(T_2 - T_1)$ is analogous to electrical voltage difference and Θ is analogous to electrical resistance.

THERMAL RESISTANCE

The thermal resistance for a given material and dimensions can be calculated:

$$\Theta = \frac{L}{4.186KA} \qquad (°C/W) \qquad (3)$$

where,

K = Thermal conductivity coefficient of the material [gm cal/(°C)(sec)(cm)]

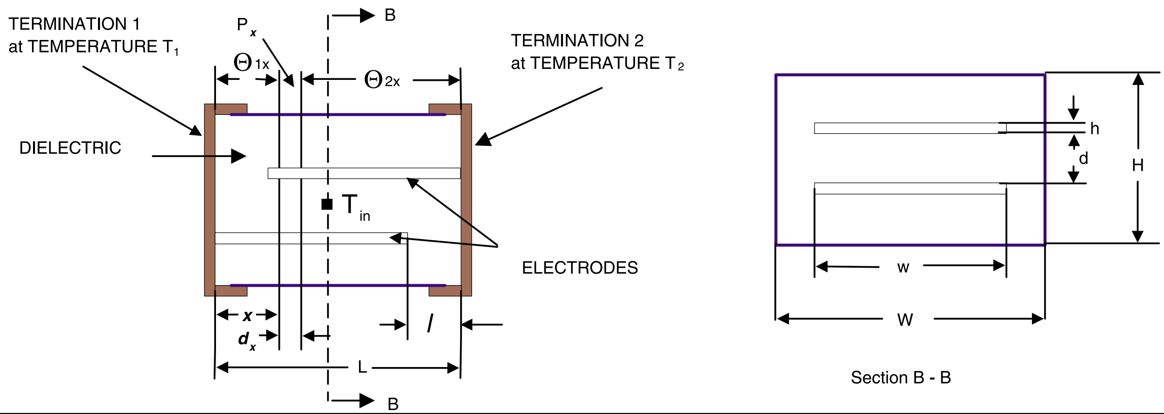
L = length of path (cm)

A = Area perpendicular to path (cm^2)

Note: When the thermal conductivity is given in watts/(°C)(cm), multiply by .2389 to obtain gm cal/(°C)(sec)(cm).

*ATC 100 series
**ATC Porcelain dielectric capacitors.

Figure 3.



To provide a useful thermal model for calculating the power dissipation of a multilayer capacitor, the following constraints are applied:

a) The thermal resistance of the terminations are negligible. This is accomplished by selection of the proper termination material, control of it's thickness, uniformity of termination deposition and tight process control.

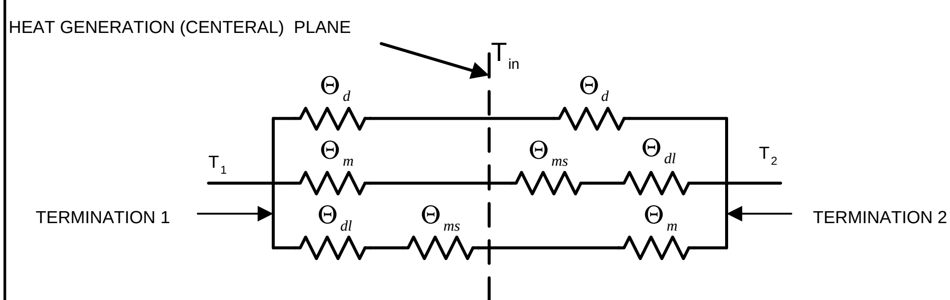
b) Heat is removed by conduction mode only, via the terminations of the capacitor to external leads or transmission lines, etc. Radiation and convection are disregarded. This constraint provides an additional safety factor in current ratings.

c) The thermal conductivity is constant over the temperature range of 25° C to 125° C.

The thermal circuit for a multilayer capacitor is complicated because there are many parallel thermal paths. Since the current varies over the length of the capacitor, the power dissipation is not concentrated at any one point in the capacitor, but is distributed throughout the length of the capacitor. To simplify this situation the equivalent thermal circuit is derived which substitutes a single lumped power dissipation source (heat generator) at the central plane of the capacitor and a lumped thermal resistance from this central plane to each of the capacitor terminations.

Figure 3 illustrates the derivation of this thermal equivalent circuit for a two electrode capacitor. A strip *dx* is selected a distance *x* from termination 1. The power dissipation in the electrodes in this strip is calculated from $i^2 R_X d_X$, where *i* is the current in one electrode at plane *x* and R_X is the resistance per unit length of the electrode. Similarly the power dissipation in the dielectric in this strip is calculated from the dissipation factor and the current. The dissipation factor of the dielectric is constant as a function of *x*. The total power dissiption in the strip *dx* is P_X and is the sum of the two above power dissipations. The thermal resistance Θ_{1X} and Θ_{2X} from the strip to the terminations consist of parallel electrode and dielectric paths and are calculated from the form:

Figure 4.



Θ_d = Thermal resistance of dielectric from Heat Generation Plane to a termination (°C/W)

Θ_m = Thermal resistance of parallel combination of all electrodes from Heat Generation Plane to the connected termination for length $= \frac{L+\ell}{2}$ (°C/W)

Θ_{ms} = Thermal resistance of parallel combination of all short electrodes from Heat Generation Plane to unconnected end of electrodes for a length $= \frac{L+\ell}{2}$ (°C/W)

$\Theta_{d\ell}$ = Thermal resistance of parallel combination of dielectric in series with short electrodes for a length $= \ell$ (°C/W)

T_{in} = Temperature of Heat Generation Plane (°C)

T1 = Temperature of termination 1 (°C)

T2 = Temperature of termination 2 (°C)

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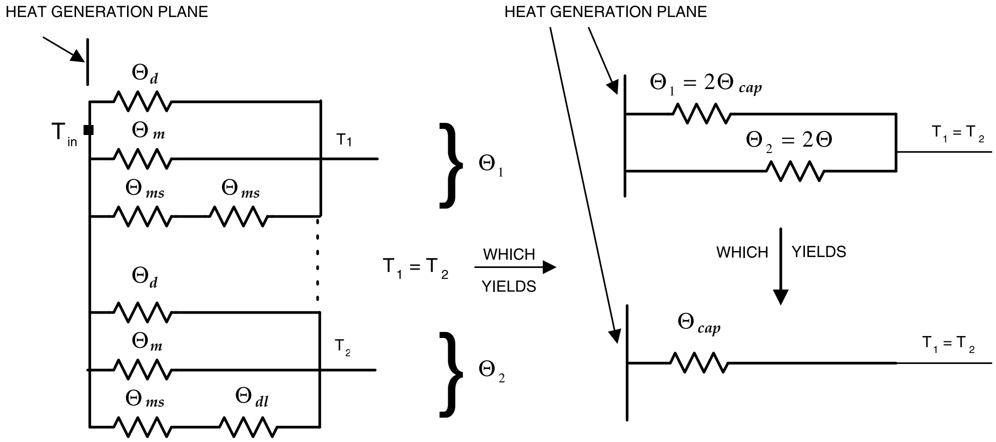
Figure 5.



$$\text{where, } \Theta_1 = \Theta_2 = 2\Theta_{cap} = \frac{1}{\left(\frac{1}{\Theta_d}\right) + \left(\frac{1}{\Theta_m}\right) + \left(\frac{1}{\Theta_{ms} + \Theta_{d\ell}}\right)} \quad (4)$$

$$\Theta_{cap} = \frac{\Theta_1 \Theta_2}{\Theta_1 + \Theta_2} \quad (5)$$

Θ_{cap} = Thermal resistance of capacitor from Heat Generation Plane to both terminations (°C/W)

$$\Theta_{1x} = \frac{x}{4.186KA} \quad or \quad \Theta_{2x} = \frac{L + \ell - x}{4.186KA}$$

If now the terminations 1 and 2 are connected together thermally but not electrically, i.e., the temperature of termination 1 is the same as the temperature of termination 2, then the temperature rise at plane *x* of the capacitor can be calculated from the expression:

$$\Delta T_X = P_X \frac{\Theta_{1X}\Theta_{2X}}{\Theta_{1X} + \Theta_{2X}}$$

where:

ΔT_X = Temperature rise above T_1 or T_2 (°C)

$\Theta_{1X} = f_1(x)$

= Thermal resistance from plane x to termination 1 (°C/W)

$\Theta_{2X} = f_2(x)\ (L + \ell - x)$

= Thermal resistance from plane x to termination 2 (°C/W)

$P_X = f_3(R_X, x, dx)$

= Power dissipated in metal electrodes and dielectric in width dx located at plane *x*

If ΔT_X is integrated, an expression is obtained in a form as follows:

$$\Delta T = f\left(P_d, \frac{\Theta}{2}\right)$$

where:

Θ = Thermal resistance from central plane to termination 1 and termination 2 (°C)

P_d = Total power dissipated in capacitor (watts)

and thus,

ΔT = Temperature rise of central plane above termination (°C).

This permits the establishment of the equivalent circuit with all the power dissipation in the central plane and thermal resistances from that plane to each of the terminations.

The validity of this result is also apparent from the symmetry of the structure of the capacitor on either side of the central plane. This symmetry is also true for the capacitor's power dissipation and thermal resistances.

Figure 4 is the thermal equivalent circuit for the two electrode capacitor in Figure 3. From Figure 4, one can see that there are two equal thermal paths from the central plane to each of the terminations. For *each* path there are *three* thermal resistances in parallel. One is metal, the second is dielectric and the third is metal in series with a small length (ℓ) of dielectric.

The first and third are through the cross-sectional area of the electrodes (wh) and the other is through the area of the dielectric (WH - 2wh). If there are N electrodes, these become Nwh/2 and (WH–.

If termination 1 is thermally connected, but not necessarily electrically connected to termination 2, T_1 becomes equal to T_2. This is equivalent to folding Figure 4 at the Heat Generation Plane and connecting termination 1 to termination 2.

The thermal resistance of the capacitor is thus developed as shown in Figure 5.

Using the equivalent circuit of Figure 5 and equations 3, 4 and 5 the thermal resistance of ATC 100A 1.0 pF and 100 pF capacitors and ATC 100B 1.0 pF, 100 pF and 1000 pF capacitors can be calculated. The results are shown in Table 1.

Θ_{cap} Calculated from Electrode and Dielectric Dimensions and Thermal Conductivity

	SERIES	100A		100B		
		ELECTRODES				
ELECTRODES	Cap Value (pF)	1	100	1	100	1000
	N = Number of Electrodes	2	28	2	18	62
	$L_{(cm)}$	0.1		0.22		
	ℓ (cm)	0.04		0.06		
	A_m (cm²)	0.00006		0.000141		
	$N A_m$ (cm²)	0.00012	0.00168	0.000282	0.02538	0.00874
	K_m	0.167 gm cal/(sec)(°C)(cm)				
	Θ_m (°C/W)	1670	120	1420	158	46
	Θ_{ms} (°C/W)	715	51	812	90	26
		DIELECTRIC				
DIELECTRIC	$L + \ell$ (cm)	0.14		0.28		
	A_{cap} (cm²)	0.02		0.07		
	A_d	0.01988	0.0183	0.06972	0.06746	0.06126
	K_d	0.03 gm cal/(sec)(°C)(cm)				
	Θ_d (°C/W)	28	30	16	16.5	18
	$\Theta_{d\ell}$ (°C/W)	5310	380	3390	376	109
		CAPACITOR				
CAP	Θ_{cap} (°C/W)	13.7	11.4	7.9	7.2	5.9

subscript d = dielectric   subscript m = metal electrode

TABLE 1

Equations used in calculation are from equations 3, 4 and 5:

$$\Theta_m = \frac{0.5\,(L+\ell)}{4.186K_m\left(\frac{NA_m}{2}\right)} \qquad \Theta_d = \frac{0.5\,(L+\ell)}{4.186K_dA_d} \qquad \Theta_{ms} = \frac{0.5\,(L-\ell)}{4.186K_m\left(\frac{NA_m}{2}\right)}$$

$$\Theta_{d\ell} = \frac{\ell}{4.136K_d\left(\frac{NA_m}{2}\right)} \qquad \Theta_{cap} = \frac{0.5}{\left(\frac{1}{\Theta m}\right)+\left(\frac{1}{\Theta d}\right)+\left(\frac{1}{\Theta ms + \Theta d\ell}\right)}$$

$A_m = wh \quad A_{cap} = WH \quad A_d = WH - whN$

NOTE: Θ_{cap} PLAYS THE SAME ROLE FOR CAPACITORS AS Θ_{jc} PLAYS FOR TRANSISTORS.

POWER RATING

As previously stated, the allowable power dissipation can be determined by the knowledge of the thermal resistance Θ_{cap}, the equivalent series resistance ESR of the capacitor, the maximum allowable internal temperature and the maximum temperature that solder or epoxy on the termination can tolerate without destruction.

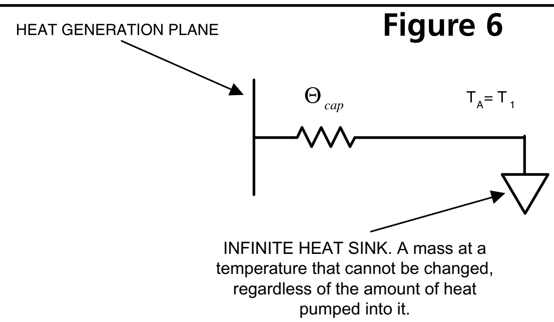
The simplified equivalent thermal circuit, *when the capacitor terminations are connected to an infinite heat sink,* is shown in Figure 6. The thermal equation for the circuit in Figure 6 is given by:

$$\Theta_{cap}\,(P_d) = (t_{in} - T_1) \qquad (6)$$

and is plotted in Figure 7.

If the vertical scale name is changed from power dissipation Pd to power dissipation allowed Pda, this curve is really a maximum power rating curve for the capacitor, where the allowed internal temperature Tin is equal to T_{1max} = 125° C.

Figure 6



where, P_d = Power dissipated in capacitor (watts)

T_A = Ambient temperature (° C)

∇ = INFINITE HEAT SINK (a mass at a temperature that cannot be changed, regardless of the amount of heat pumped into it)

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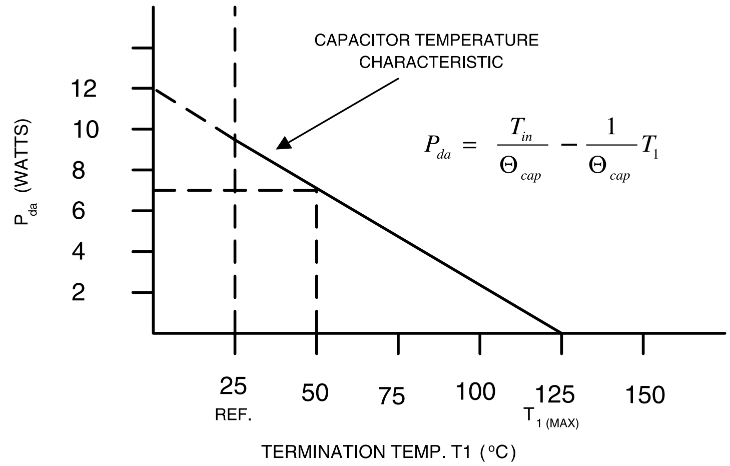
Figure 7.



where, at $T_A = T_1 = 25°C$; $P_{d_{max}} = \left(\frac{1}{\Theta_{cap}}\right) T_{in}$

and at $P_d = 0$; $T_{1_{max}} = 125°C$

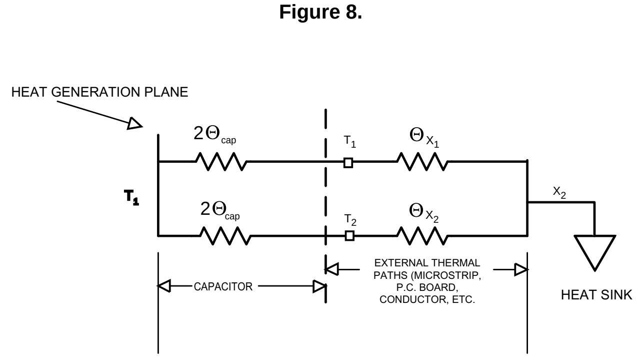
slope $= \frac{\Delta P_d}{\Delta T_1} = -\frac{1}{\Theta_{cap}}$

where, P_{da} = Power dissipation allowed for an internal temperature of T_{1max}

For example, if the heat sink and therefore, the terminations are set to 50° C, then the internal temperature will be 125° C for a P_{da} of 7.2 watts. This is the particular condition shown by the dotted lines in Figure 7. Similarly, one can determine the power rating of the capacitor for any given heat sink temperature of termination temperature. It should be stressed that this equivalent circuit and curve is for the specific condition where terminations are connected to an infinite heat sink. Values of P_{da} for actual capacitors are plotted in power temperature rating curves 1 and 2.

Curve 6 provides power dissipation and thermal resistance for both 100A and 100B, for capacity values between 1.0 pF and 1000 pF.

Figure 8.



Θ_{x1} = External thermal resistance, from termination 1 to heat sink (°C/W)

Θ_{x2} = External thermal resistance, from termination 2 to heat sink (°C/W)

The allowable power dissipation for the capacitors in Table 1 with an infinite heat sink at 25° C connected to the termination is given in Table 2.

The thermal situation taking into account external thermal resistance is shown in Figure 8.

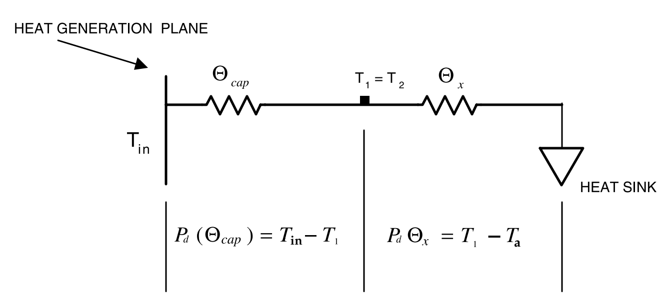
Assuming that $T_1 = T_2$, the thermal circuit becomes Figure 9.

The thermal circuit is described by:

$$P_d\Theta_{cap} + P_d\Theta_x = T_{in} - T_A \quad (8)$$

Since Tin is a maximum of 125°C and both Θ_{cap} and Θ_x are known, the circuit designer can solve for the maximum allowable Pda either algebraically or graphically. To solve

Figure 9.



where, $\Theta_x = \frac{\Theta_{x1}\Theta_{x2}}{\Theta_{x1} + \Theta_{x2}} \quad (7)$

Infinite Heat Sink @ 25°C connected to terminations					
Series	100A		100B		
Cap value (pF)	1	100	1	100	1000
Θ_{cap} (°C/W)	13.7	11.4	7.9	7.2	5.9
Max Power Diss. (watts) at 25°C	7.3	8.8	12.6	13.9	16.9

Table 2

graphically, use Figure 7 and superimpose:

$$P_d = \frac{1}{\Theta_x} (T_1 - T_A) \qquad (9)$$

This is shown in Figure 10.

Starting at $T_1 = T_A$, plot a line whose slope is $^1/\Theta_x$; the intersection of the two lines gives the allowed power dissipation and the actual termination temperature for this thermal circuit. The internal temperature (T_{in}) is 125°C.

CURRENT RATINGS

Knowing the allowed power dissipation (P_{da}) in the capacitor, for a given external thermal path, and knowing ESR at the frequency of interest, the dissipation limited current can then be calculated:

$$I_{DL} = \sqrt{\frac{P_{da}}{ESR}} \qquad (10)$$

ESR values can be obtained from ATC performance curves on page 12.

I_{DL} is valid as long as the maximum rated voltage of the capacitor is not exceeded. The voltage limited current due to the maximum rated voltage is calculated from Equation 11.

$$I_{VL} = \frac{E_{rated}}{X_c} = E_{rated} \; (2\pi f C) \qquad (11)$$

A plot of maximum allowable current vs. capacitance from equations (10) and (11) results in a family of curves as shown in Figure 11. From Figure 11, it is clear that when I_{VL} becomes smaller than I_{DL}, I_{VL} becomes the rated current. See current rating curves 3, 4 and 5 for 100A and 100B capacitors.

Conclusion

Information and methods for arriving at RF current ratings of multilayer monolithic ceramic capacitors have been presented. It has been shown that the general shape of the current rating curves can be established. Expressions for the effect of various capacitor parameters (such as Equivalent Series Resistance, RF Voltage Rating and Thermal Resistance), on the current ratings have been developed. This data was developed theoretically and then verified experimentally. Examples of how to use this information to arrive at current ratings for specific thermal conditions have been included.

Figure 10.

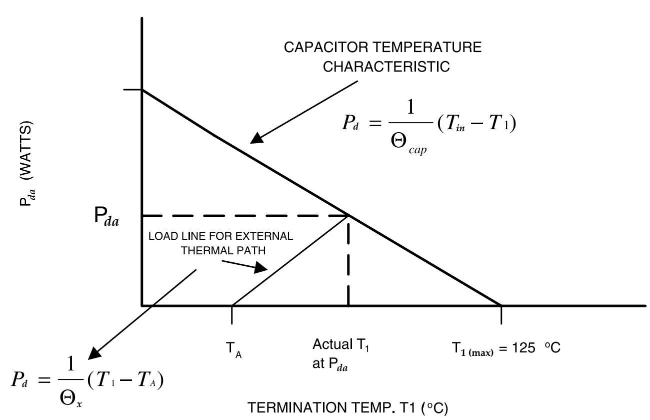
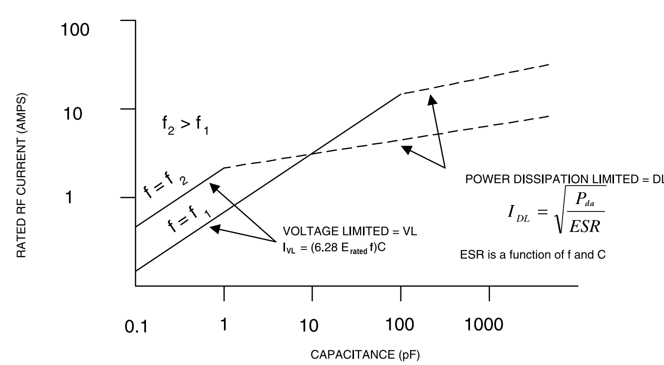


Figure 11.



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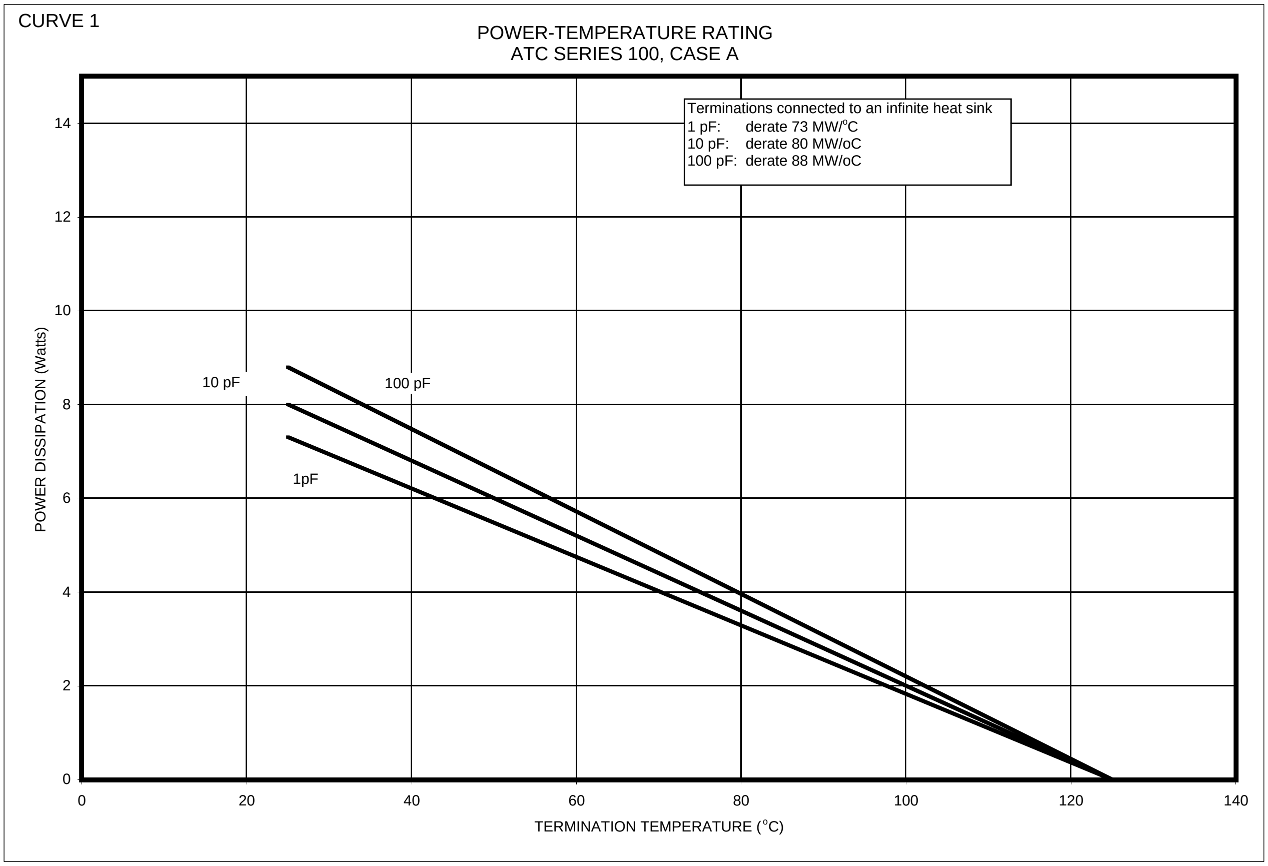
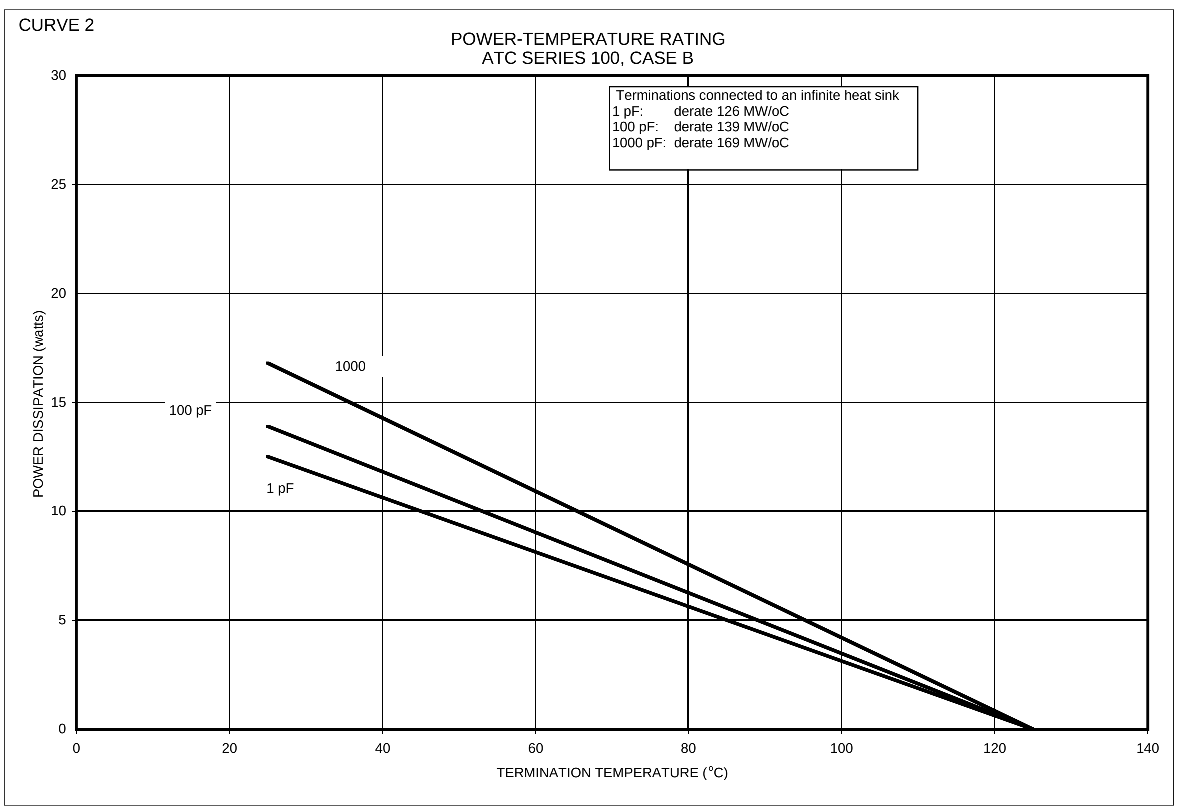
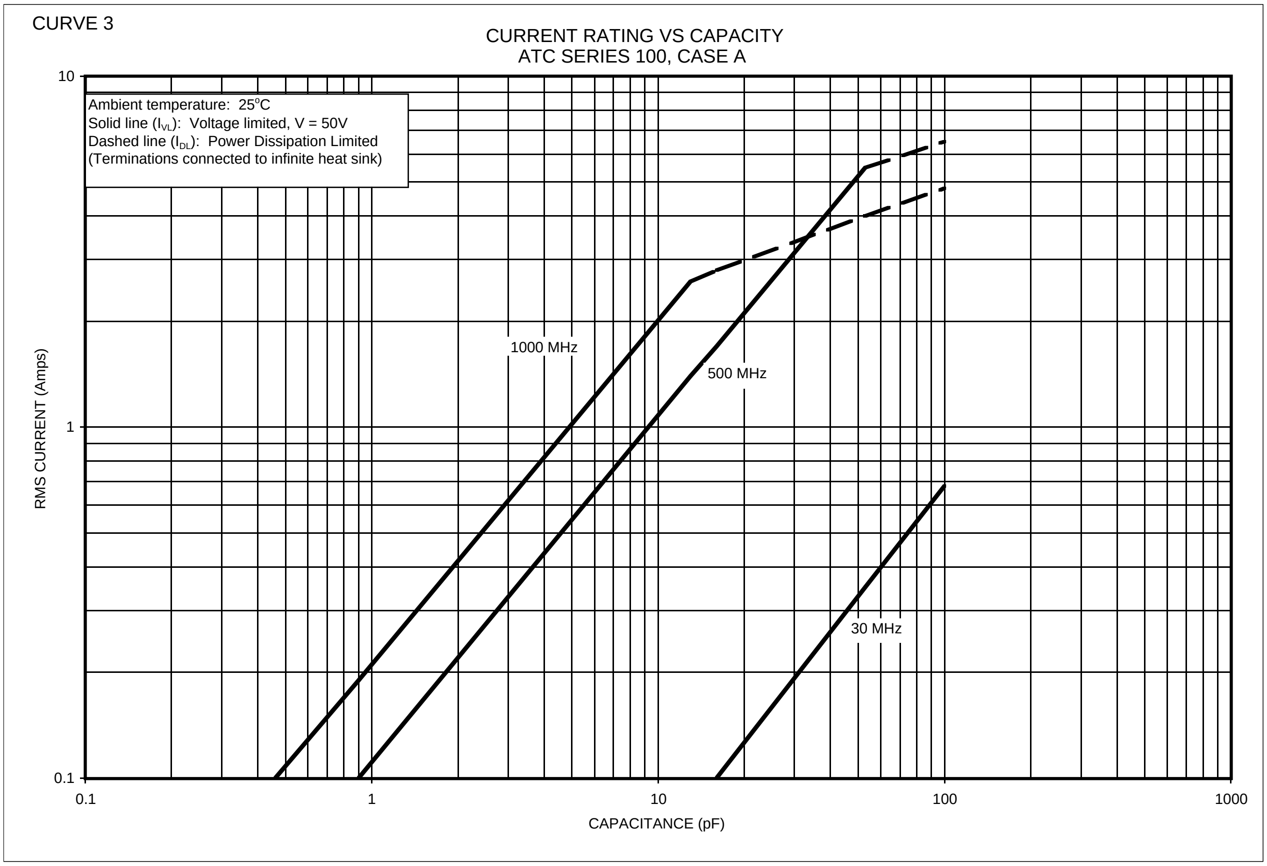
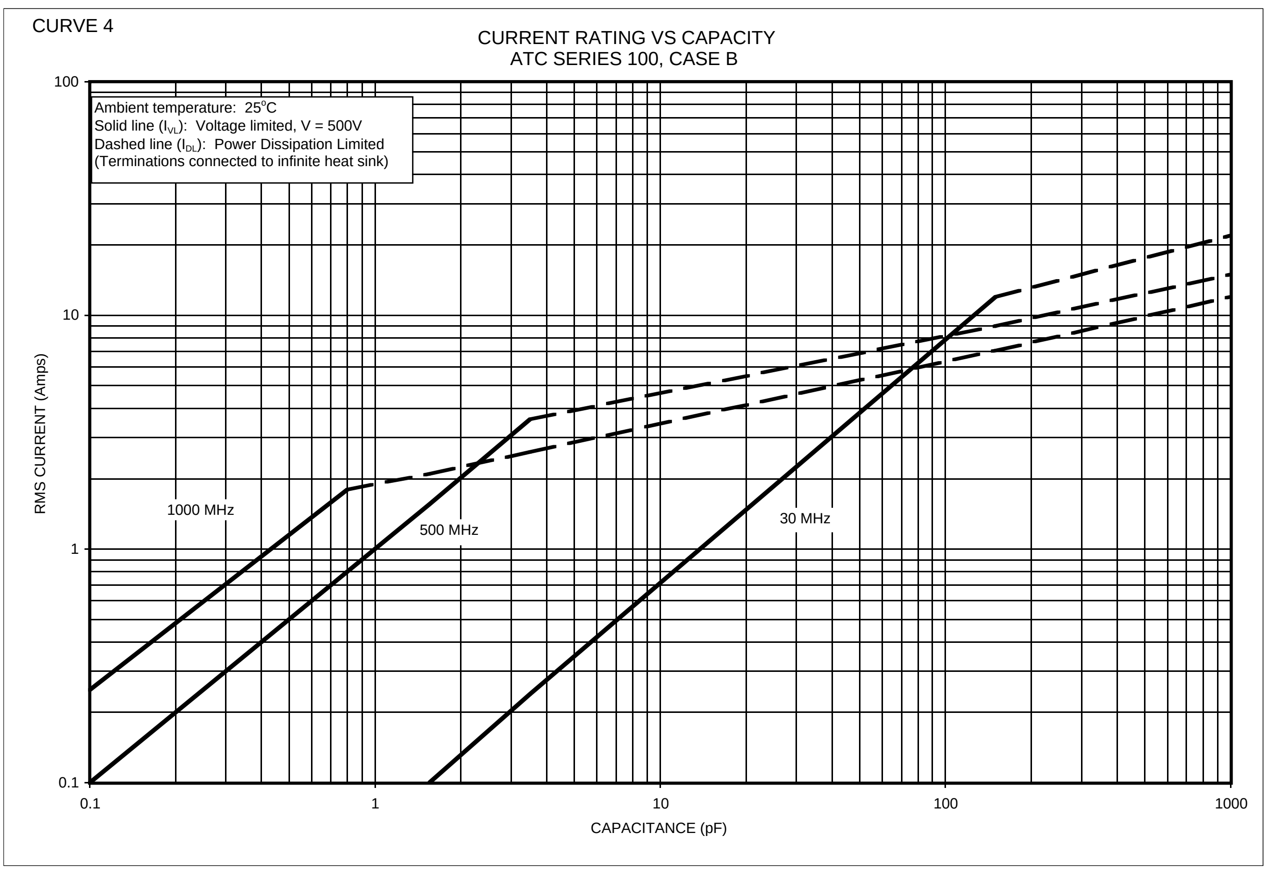

CURVE 1
POWER-TEMPERATURE RATING
ATC SERIES 100, CASE A
Terminations connected to an infinite heat sink
1 pF: derate 73 MW/°C
10 pF: derate 80 MW/oC
100 pF: derate 88 MW/oC
10 pF
100 pF
1pF
POWER DISSIPATION (Watts)
TERMINATION TEMPERATURE (°C)
0
2
4
6
8
10
12
14
20
40
60
80
100
120
140


CURVE 2
POWER-TEMPERATURE RATING
ATC SERIES 100, CASE B
Terminations connected to an infinite heat sink
1 pF: derate 126 MW/oC
100 pF: derate 139 MW/oC
1000 pF: derate 169 MW/oC
1000
100 pF
1 pF
POWER DISSIPATION (watts)
TERMINATION TEMPERATURE (°C)
0
5
10
15
20
25
30
20
40
60
80
100
120
140





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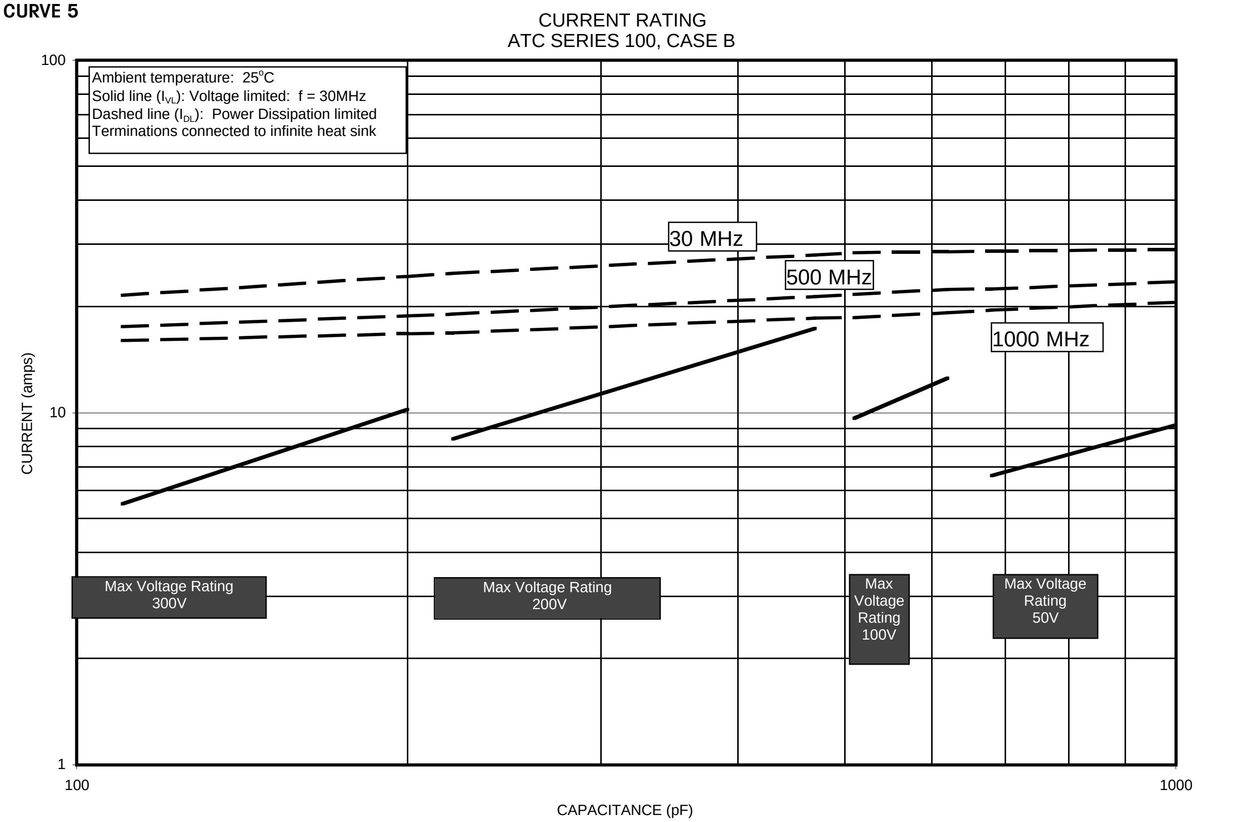
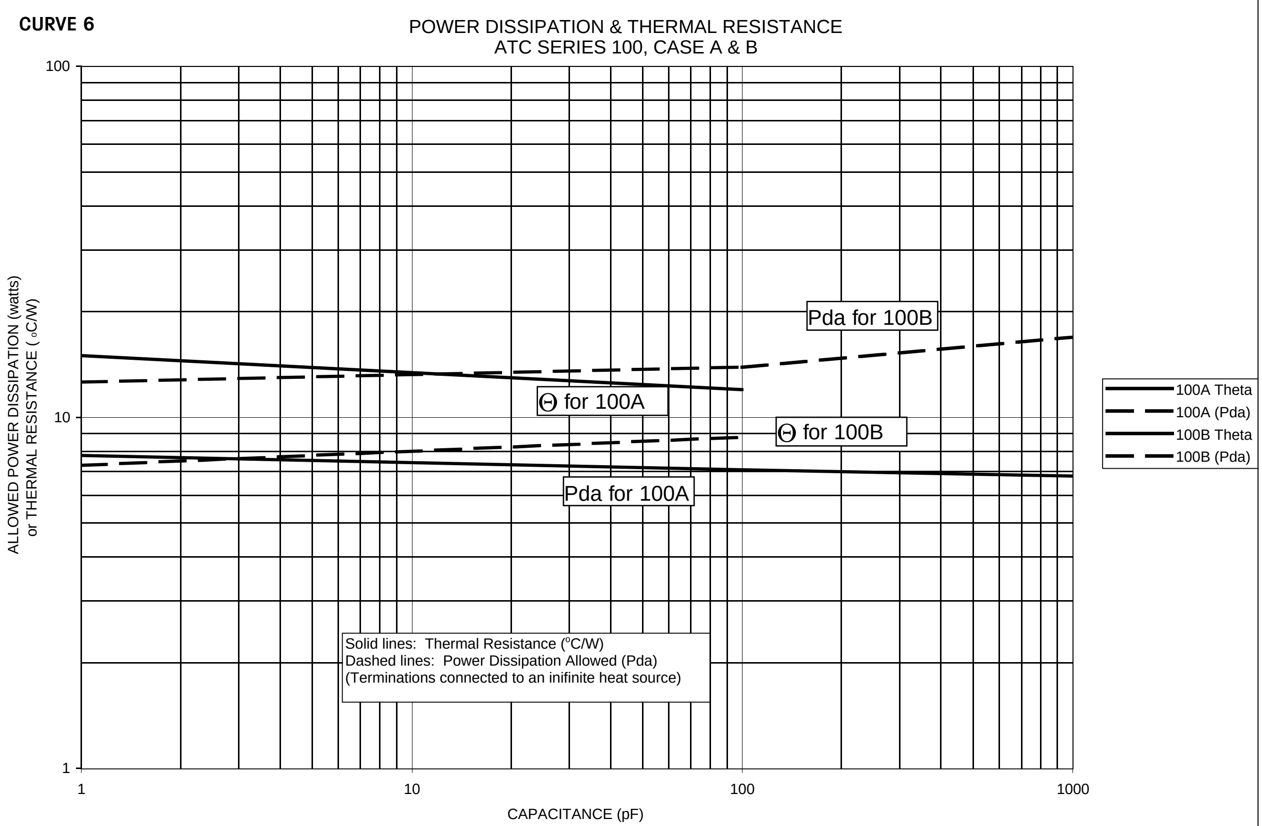
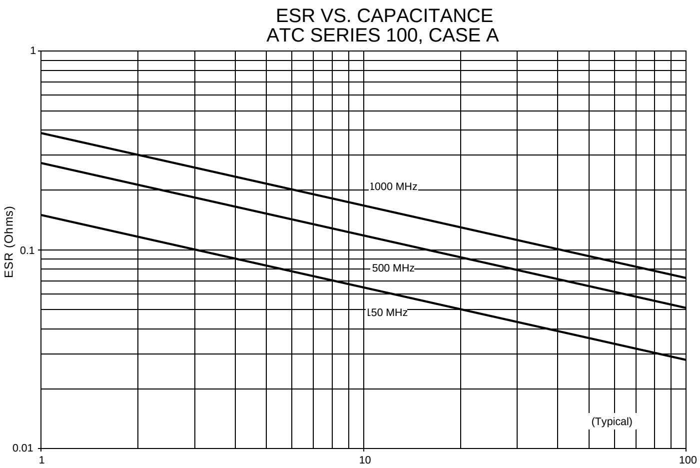
CURVE 5



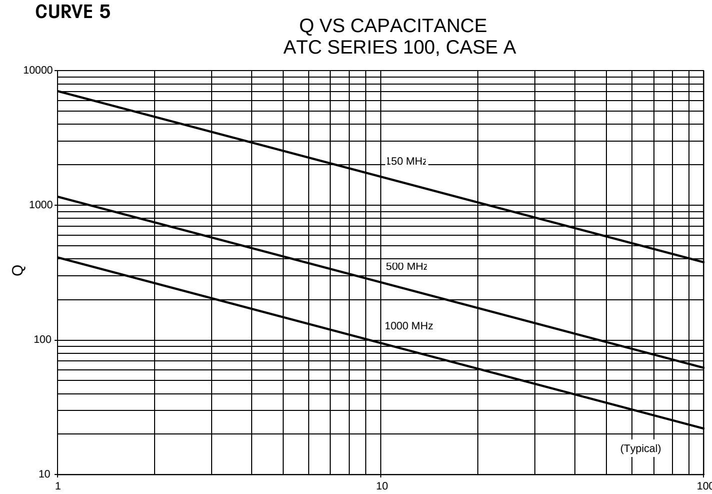
CURVE 6



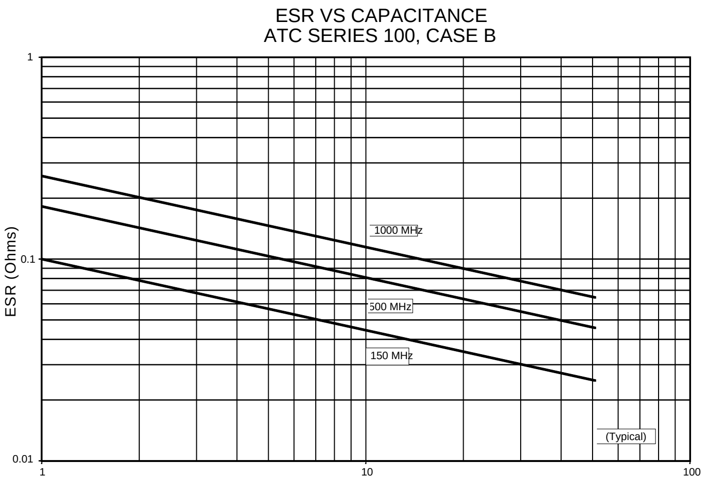
CURVE 5



CURVE 5



CURVE 5



CURVE 5